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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DU, THUAN N	

ART UNIT	PAPER NUMBER
2116	

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DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,822	ZILKA, ANTHONY M.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20041209* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12 and 20-30, drawn to active/idle mode processing of a computer system based on detected events, classified in class 713, subclass 323.

II. Claims 13-19, drawn to active/idle mode processing of a processor, classified in class 713, subclass 323.

3. The inventions are distinct, each from the other because: inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the invention of Group I is transitioning a processor of a computer system into a reduced power mode and/or normal mode based on detected events. The subcombination has separate utility such as a power control circuit is included in a processor.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

5. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Ed Taylor, Reg. No. 25,129, on December 9, 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-12 and 20-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 13-19 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, 8, 11, 12 and 20-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iacobovici et al. [Iacobovici] (U.S. Patent No. 6,704,876).

9. Regarding claim 1, Iacobovici teaches a method comprising:

detecting a first event (estimated CPU power dissipation is greater than PHWM value) that allows for lower performance in a processor [col. 4, lines 5-10];

transitioning said processor from a high performance state to a low performance state upon detection of said first event [col. 4, lines 11-14];

detecting a second event (estimated CPU power dissipation is smaller than PLWM value) that can utilize greater performance in said processor [col. 4, lines 15-21]; and

transitioning said processor from said low performance state to said high performance state upon detection of said second event [col. 4, lines 21-22].

Iacobovici does not explicitly teach that the occurrence of the first event is predicted. However, Iacobovici teaches that the power dissipation of the CPU is *estimated*, not 100 percent accurate. Therefore, one of ordinary skill in the art would have recognized that Iacobovici obviously predicts when the CPU could be slowed down.

10. Regarding claim 2, Iacobovici teaches that cache miss event is detected [col. 2, lines 60-62].

11. Regarding claim 3, Iacobovici teaches that cache miss event causes the CPU to fetch data from external memory [col. 2, lines 62-64].

12. Regarding claim 4, Iacobovici teaches that the incoming data from the memory fetch is detected [col. 4, lines 38-43].

13. Regarding claim 5, Iacobovici teaches that cache miss event causes the CPU to stall instruction pipeline (CPU is pipeline-based) [Fig. 4; col. 3, line 21-22].

14. Regarding claim 6, Iacobovici teaches that CPU signal (CPU operation) is monitored [in order to estimate the power dissipation of the CPU, the operation of the CPU must be monitored].

15. Regarding claim 8, Iacobovici teaches that high performance state consumes a greater amount of power than low performance state [col. 1, lines 51-62].

16. Regarding claim 11, Iacobovici teaches that the transitioning from a high performance state to a low performance state further comprises slowing down an internal processor core clock signal from a normal operating frequency to a lower frequency [col. 4, lines 10-13].

17. Regarding claim 12, Iacobovici teaches that the transitioning from said low performance state to said high performance state comprises speeding up said internal processor core clock signal to said normal operating frequency [col. 4, lines 21-23].

18. Regarding claims 20-25, Iacobovici teaches the claimed method steps. Therefore, Iacobovici teaches the apparatus to implement the claimed method steps.

19. Regarding claims 26-30, Iacobovici teaches the claimed method steps. Therefore, Iacobovici teaches the instructions stored in a machine readable medium for carrying out the claimed method steps.

20. Claims 7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iacobovici et al. [Iacobovici] (U.S. Patent No. 6,704,876) and Kardach et al. [Kardach] (U.S. Patent No. 6,014,751].

21. Regarding claims 7, 9 and 10, Iacobovici teaches that the CPU comprises a plurality of functional units [Fig. 4; col. 3, lines 34-65]. Iacobovici does not explicitly teach that those functional units could be selectively powering down and powering up.

Kardach teaches a processor (processor 14 of Figs. 4, 5) comprises a plurality of functional units, wherein the functional units could be selectively powering down [col. 5, lines 49-63; col. 4, lines 5-8, 40-49].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Iacobovici to power down and power up selected functional

units as taught by Kardach because it would reduce the power consumption of the CPU and maintain the cache coherency of the system.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday and Wednesday-Friday: 9:30 AM - 8:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (703) 872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
December 9, 2004